~~DEVICE AND METHOD FOR CONVERTING DATA SEQUENCES
BETWEEN FR FORMAT AND ATM FORMAT~~

The asynchronous transfer modus (ATM) serves as a basis for a

5 universal and international broadband communication, whose configuration

~~ari [sic]~~ standardized by means of the ATM forum found in the year 1991.

The asynchronous transfer modus is an asynchronous time-division

multiplexer method, which enables an integration of different communication

services, such as voice communication, data communication, video

10 telephone, video communication etc. given an arbitrary scaling ability of the

transmission capacity. The structure of a typical ATM cell is represented in

Rathgeb, Wallmeier, page 79, for example.

Network accesses having transmission rates of 64 kbit/s up to 45

Mbit/s are enabled by means of "Frame Relay", whereby the data frames can

15 have a variable length up to 8 kbytes. FR network accesses are particularly

suitable for the ~~data~~ communication (~~internet, for example~~) e.g. in the Internet. The

specifications are standardized by means of the FR forum. The structure of

an FR frame is described in Rathgeb, Wallmeier, page 269 through page

271, for example.

20 The conversion of data sequences between FR and ATM format

("interworking") can be carried out as a ~~what is referred to as~~ network

interworking, ~~whereby~~ in which the FR frames are directly converted into

corresponding ATM frames and vice-versa or can be carried out by means of

a ~~what is referred to as service interworking~~ "service interworking", whereby the content of the FR

25 frames are converted into an AAL5 (ATM adaption layer 5) cell stream. The

network interworking is described in FR forum document No. FRF. 5 and the

service interworking is described in FR forum document No. FRF. 8.

Given the transmission from one format to the other one, the

frames must be frequently translated in their control data area (header),

30 particularly regarding the service interworking. For this purpose, the frames

of an FR connection that are supplied via the interfaces are stored in the main memory of the central computer (frame processor FP) of the conversion device. For this purpose, the central computer reads in the data from the appertaining interface (such as E1/DS1 in the FR interface module) by means

5 of read commands or by means of a direct memory access (DMA). Subsequent to the processing by means of the central computer, the frames are given to a further processing interface, such as an ATM communication module (segmentation and reassembly sub-layer SAR), by means of write commands or by means of a direct memory access. This method has the

10 disadvantage that the central computer cannot continue to work and that the program running on it must be interrupted during the transmission of the data to and from the main memory of the central computer. Therefore, the throughput rate of the conversion device is significantly reduced. Long FR frames hold up the central computer with waiting times as much as short FR

15 frames intensively load it with respect to the processing time.

SUMMARY OF THE INVENTION

Therefore, the invention is based on the object of proposing a device and a method for converting data sequences between FR format and ATM format, in which the throughput rate is increased.

The object is achieved by a conversion device, which

20 comprises an FR communication module for connecting to an FR communication link, an ATM communication link, a central computer for controlling the FR communication module and the ATM communication module and a buffer memory, which is connected to the central computer, the FR communication module and the ATM communication module via an

25 internal communication link.

Given the conversion of the data sequences from FR into the ATM format and vice-versa, the data (usage data and control data) are not stored in the memory of the central computer but in the buffer memory, which is connected to the FR communication module and the ATM communication module via a separate internal communication link. As a result, the

30

operation of the central computer need not be interrupted during the readin and readout of the data. Therefore, the data throughput rate is clearly increased. The process of the data transmission between the communication modules and the buffer memory is also controlled via the

5 central computer. However, this control function contributes only to a small increase in work load of the central computer.

Preferably, the communication modules, the buffer memory and the central computer are connected via a bus link, particularly via a high-capacity PCI bus. A separate bus link can also be provided for

10 each of the communication modules.

For purposes of achieving a further increase of the throughput rate, it is possible to divide the buffer memory into two units, whereby one unit is fashioned for storing the data for the further processing in the FR communication module and the other unit for storing data for the further

15 processing in the ATM communication module. The utilization of two separate central computers is advantageous, in which each computer is respectively responsible for one "communication direction".

BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments of the present invention are described on the basis of the enclosed drawings.

20   Figure 1 is   a schematic representation of a first exemplary embodiment of the inventive conversion device;

Figure 2 is   a schematic illustration of a second exemplary embodiment of the inventive conversion device;

25   Figure 3 is   a schematic illustration of a third exemplary embodiment of the inventive conversion device;

Figure 4 ~~is~~ a schematic representation of a fourth

exemplary embodiment of the inventive

conversion device and

Figure 5 ~~is~~ a schematic representation of a fifth exemplary

embodiment of the inventive conversion

device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a first exemplary embodiment of the inventive

conversion device. In this example, eight communication links of the type

E1/DS1 (transmission capacity 2.048 Mbit/s or, respectively, 1.544 Mbit/s are

connected to the FR communication module. However, arbitrary other

communication links that are possible in the FR standard can be utilized.

The FR communication module PIM (Physical Interface Module) consists of

two functional modules, the physical interface PHY and the FR control FRCC

(Frame Relay Communication ~~Controller[sic]~~ Controller). The FR communication

module PIM is connected via a PCI (Peripheral Component Interconnect) bus

to the ATM communication, which, in turn, consists of the

segmentation/chaining unit SAR, ~~whereby~~ by which the AAL5 (ATM Adaption Layer)

functionality is implemented ~~therein~~ within, and consists of the ATM adaptation layer

ALM, which are connected to one another via ~~an~~ a utopia (Universal Test and

Operations Physical Interface for ATM) interface. The buffer memory PSSM

(PIM SAR Shared Memory), which comprises a dynamic direct access memory

(DRAM) and an appertaining memory controller, is also connected to the PCI

bus. Besides, the central computer FP, which, for example, can comprise a

~~Risk~~ RISC ~~risk~~ CPU, a system control, a storage unit, a clock control etc., is connected

to the PCI bus.

The second exemplary embodiment of the inventive conversion

device shown in Figure 2 only differs from the first exemplary embodiment in

that separate bus links are provided between the FR communication module and the

buffer memory, on one hand, and between the ATM communication module and the

buffer memory, on the other hand. Both bus links are connected to the

central computer FP, which controls the data transmission processes on the
bus links.

In the third exemplary embodiment of the inventive conversion
device schematically shown in Figure, the buffer memory PSSM is divided

5   into two units for purposes of further enhancing the performance, whereby
the first unit serves the purpose of transmitting from the FR side to the ATM
side and the second unit serves the purpose of transmitting from the ATM
side to the FR side.

In the fourth exemplary embodiment of the inventive conversion

10   device shown in Figure 4, the FRCC module in the FR communication
module PIM and the SAR module in the ATM communication module are also
fashioned in a two-piece manner, whereby respectively one part is
responsible for one transmission direction. Therefore, a further increase in
speed can be achieved, whereby, on the other hand, the constructional

15   outlay increases, too.

The conversion device of the third exemplary embodiment, which is
shown in Figure 5, additionally contains separate bus links for the readin
process into the buffer memory PSSM, on one hand, and for the readout
process from the buffer memory, on the other hand. For both transmission

20   directions, the readin and readout process therefore can be carried out
independently of one another, so that a further enhancement of the
transmission performance is enabled.

The method of functioning of the conversion devices that are
schematically shown in Figures 1 through 3 is explained in the following. FR

25   data sequences are read from the physical interfaces by the FR
communication module PIM and then are stored in the buffer memory PSSM
upon control by means of the central computer FP. Subsequently, the data
are read-in the ATM communication module, upon control by means of the
central computer again, via the PCI bus. The segmentation/chaining unit

30   SAR carries out the interconnecting of the header data and the chaining of

the data to be transmitted into ATM cells, which are supplied via the utopia interface of the ATM adaptation layer - processing unit ALM and are made available there at output terminals Y_b, for the further processing in a coupling field, for example.

5   Given the reversed conversion, the data sequences get in the ATM format from the ATM adaptation layer - processing unit, via the utopia interface, to the segmentation chaining unit SAR, in which the ATM cells are chained and are stored via the bus link into the buffer memory PSSM. From there, the data are read-in via the FR communication module

10   PIM, are converted into the FR format with frames of variable length, and are subsequently supplied to one of the physical interfaces.

As a result of the temporary storing of the converted data via the internal communication link in the buffer memory, an interruption of the operation of the central computer FP is not required when the data are read-

15   in/readout. The control of the readin/readout process, on one hand, the translation of the FR headers in the network IW case and, on the other hand, the conversion in the service IW case, requires only a few accesses via the PCI bus and therefore represents only a small load for the central computer. Thus, a performance enhancement of the conversion device by a factor of 2

20   through 3 and higher can be achieved.

The PCI burst capability of all connected PCI bus users and also the performance capacity of the central computer FP are conditions with respect to a high transmission performance. Although the central computer FP does not access the buffer memory PSSM too often, its conversion speed

25   must be high given the service interworking functionality.